8254 Programmable Interval Timer/Counter

The Intel 8254 is a counter/timer device designed to solve the common timing control problems in microcomputer system design. It provides three independent 16-bit counters, each capable of handling clock inputs up to 10 MHz. All modes are software programmable. The 8254 uses HMOS technology and comes in a 24-pin plastic or CERDIP package.

General

The 8254 is a programmable interval timer/counter designed for use with Intel microcomputer systems. It is a general purpose, multi-timing element that can be treated as an array of I/O ports in the system software.

The 8254 solves one of the most common problems in any microcomputer system, the generation of accurate time delays under software control.

Instead of setting up timing loops in software, the programmer configures the 8254 to match his requirements and programs one of the counters for the desired delay.

After the desired delay, the 8254 will interrupt the CPU. Software overhead is minimal and variable length delays can easily be accommodated.

Some of the other counter/timer functions common to microcomputers which can be implemented with the 8254 are:

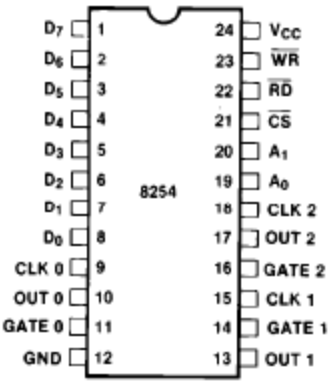
Real time clock; Event-counter; Digital one-shot; Programmable rate generator

Square wave generator; Binary rate multiplier; Complex waveform generator

Complex motor controller

Q. Explain the various signals of 8254 programmable interval timer/counter with the help of PIN Diagram.

The pin diagram of 8254 programmable timer interval/counter consist all the pins that are used to carry address, data and control signals. Address pins are required for selecting different functional blocks (i.e. counters and control register), data lines are used to act as the communication media between the 8254 and the processor. Control signals are for various purposes like read/write, and the I/O lines. These functions of these pins are described below:



Symbol	Pin	Type	Name and Function
D7-D0	1-8	I/O	Bi-directional tri state data bus.
CLK-0	9	I	Clock Input of counter 0
OUT-0	10	O	Output of counter 0

<table>
<tr><td>GATE-0</td><td>11</td><td>I</td><td colspan="3">Gate input of Counter 0</td></tr>
<tr><td>GND</td><td>12</td><td></td><td colspan="3">Power Supply Connection</td></tr>
<tr><td>Vcc</td><td>24</td><td></td><td colspan="3">+5V Power Supply connection</td></tr>
<tr><td>WR’</td><td>23</td><td>I</td><td colspan="3">Low active write enable</td></tr>
<tr><td>RD’</td><td>22</td><td>I</td><td colspan="3">Low active read enable</td></tr>
<tr><td>CS’</td><td>21</td><td>I</td><td colspan="3">Low active chip select line</td></tr>
<tr><td>A1-A0</td><td>20-19</td><td>I</td><td colspan="3">Used to select one of the three Counters or the Control Word Register for read or write operations. Normally connected to the system address bus.
A1 | A0 | Function
0 | 0 | Counter 0
0 | 1 | Counter 1
1 | 0 | Counter 2
1 | 1 | ControlWord Register</td></tr>
<tr><td>CLK-2</td><td>18</td><td>I</td><td colspan="3">Clock Input of counter 0</td></tr>
<tr><td>OUT-2</td><td>17</td><td>O</td><td colspan="3">Output of counter 0</td></tr>
<tr><td>GATE-2</td><td>16</td><td>I</td><td colspan="3">Gate input of Counter 0</td></tr>
<tr><td>CLK-1</td><td>15</td><td>I</td><td colspan="3">Clock Input of counter 0</td></tr>
<tr><td>GATE-1</td><td>14</td><td>O</td><td colspan="3">Gate input of Counter 0</td></tr>
<tr><td>OUT-1</td><td>13</td><td>I</td><td colspan="3">Output of counter 0</td></tr>
</table>

Q. Explain the functions of various components of 8254 (Programmable Interval Timer/Counter) with the help of a block diagram.

The 8254 uses HMOS technology and comes in a 24-pin plastic or CERDIP package. It is a counter/timer device designed to solve the common timing control problems in microcomputer system design. It provides three independent 16-bit counters, each capable of handling clock inputs up to 10 MHz. All modes are software programmable. Various components of the 8254 are shown in figure and aredescribed below:

- Data Bus Buffer
- Read/Write logic
- Control word Register
- Three Counters

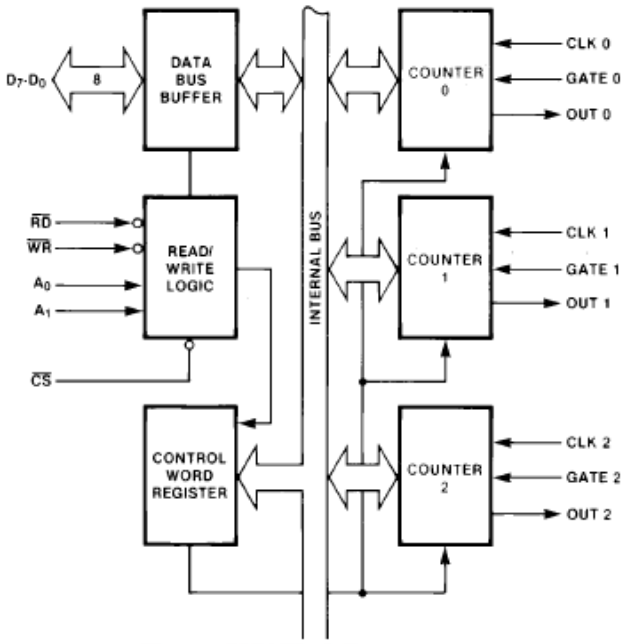


Figure: 8254 Block Duagram

1. Data Bus Buffers:

This 3-state, bi-directional, 8-bit buffer is used to interfacethe 8254 to the system bus.

2. **READ/WRITE LOGIC:** The Read/Write Logic accepts inputs from the system bus and generates control signals for the other functional blocks of the 8254. A1 and A0 select one of the three counters or the Control Word Register to be read from/written into. A ``low'' on the RD input tells the 8254 that the CPU is reading one of the counters. A ``low'' on the WR input tells the 8254 that the CPU is writing either a Control Word or an initial count. Both RD and WR are qualified by CS. RD and WR are ignored unless the 8254 has been selected by holding CS low.
3. **CONTROL WORD REGISTER:** The Control Word Register is selected by the Read/Write Logic when A1,A0 = 11. If the CPU then does a write operation to the 8254, thedata is stored in the Control Word Register and isinterpreted as aControl Word used to define theoperation of the Counters.The Control Word Register can only be written to;status information is available with the Read-BackCommand.
4. **COUNTER 0, COUNTER 1, COUNTER 2:** The 8254 has three identical but fully independent Counters. These are 16-bit pre-settable synchronous down counter. Each Countermay operate in a different Mode. The contents of Control Word Register determinehow the Counter operates.The status register, whenlatched, contains the current contents of the ControlWord Register and status of the output and nullcount flag.

Q. Describe the Control Word (and the read/write) operation of 8254 programmable interval timer/counter:

Counters are programmed by writing a Control Word and then an initial count. The Control Words are written into the Control WordRegister, which is selected when A1,A0 = 11. The Control Word itself specifies which Counter is being programmed.

8254 Control Word Format

$A_1,A_0 = 11$ $\overline{CS} = 0$; $\overline{RD} = 1$ $\overline{WR} = 0$

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC - Select Counter

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Read-Back Command (see Read Operations)

M - Mode

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

R/W - Read/Write

RW1	RW0	
0	0	Counter Latch Command (see Read Operations)
0	1	Read/Write least significant byte only
1	0	Read/Write most significant byte only
1	1	Read/Write least significant byte first, then most significant byte

BCD

0	Binary Counter 16-bits
1	Binary Coded Decimal (BCD) Counter (4 Decades)

Note : Don't xare(X) terms should be zero '0' for compatibility

By contrast, initial counts are written into the Counters, not the Control Word Register. The A1,A0 inputs are used to select the Counter to be written into. The format of the initial count is determined by the Control Word used.

Write Operations

The programming procedure for the 8254 is very flexible. Only two conventions need to be remembered:

1) For each Counter, the Control Word must be written before the initial count is written.

2) The initial count must follow the count format specified in the Control Word (least significant byte only, most significant byte only, or least significant byte and then most significant byte).
Since the Control Word Register and the three Counters have separate addresses (selected by the A1,A0 inputs), and each Control Word specifies the Counter it applies to (SC0,SC1 bits), no special instruction sequence is required. Any programming sequence that follows the conventions in figure of control word (given above) is acceptable.
A new initial count may be written to a Counter at any time without affecting the Counter's programmed Mode in any way. Counting will be affected as described in the Mode definitions. The new count must follow the programmed count format.

Read Operations

It is often desirable to read the value of a Counter without disturbing the count in progress. This is easily done in 8254.
There are three possible methods for reading the counters: a simple read operation, the Counter Latch Command, and the Read-Back Command. Each is explained below.

i. A simple read operation

The first method is to perform a simple read operation. To read the Counter, which is selected with the A1, A0 inputs, the CLK input of the selected Counter must be inhibited by using either the GATE input or external logic. Otherwise, the count may be in the process of changing when it is read, giving an undefined result.

ii. COUNTER LATCH COMMAND

The second method uses the ``Counter Latch Command''. Like a Control Word, this command is written to the Control Word Register, which is selected when A1,A0 = 11. Also like a Control Word, the SC0, SC1 bits select one of the three Counters, buttwo other bits, D5 and D4, distinguish this command from a Control Word.

Figure : Counter Latch Command Format

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	0	0	X	X	X	X

SC1, SC0 - Specify the counter to be latched

SC1	SC0	COUNTER
0	0	0
0	1	1
1	0	2
1	1	Read Back Command

Note: Don't Care must be zero '0'

The selected Counter's output latch (OL) latches the count at the time the Counter Latch Command is received. This count is held in the latch until it is read by the CPU (or until the Counter is reprogrammed). The count is then unlatched automatically and the OL returns to ``following'' the counting element (CE). This allows reading the contents of the Counters ``on the fly'' without affecting counting in progress. Multiple Counter Latch Commands may be used to latch more than one Counter. Each latched Counter's
Output latch (OL) holds its count until it is read. Counter Latch Commands do not affect the programmed Mode of the Counter in any way. If a Counter is latched and then, some time later, latched again before the count is read, the second Counter Latch Command is ignored. The count read will be the count at the time the first Counter Latch Command was issued.
With either method, the count must be read according to the programmed format; specifically, if the Counter is programmed for two byte counts, two bytes must be read. The two bytes do not have to be read one right after the other; read or write or programming operations of other Counters may be inserted between them.
Another feature of the 8254 is that reads and writesof the same Counter may be interleaved; for example,if the Counter is programmed for two byte counts, the following sequence is valid.
1) Read least significant byte.
2) Write new least significant byte.
3) Read most significant byte.
4) Write new most significant byte.

If a Counter is programmed to read/write two-bytecounts, the following precaution applies: A programmust not transfer control between reading the first and second byte to another routine which also readsfrom that same Counter. Otherwise, an incorrectcount will be read.

iii. READ-BACK COMMAND

The third method uses the Read-Back Command.This command allows the user to check the countvalue, programmed Mode, and current states of theOUT pin and Null Count flag of the selected counter(s).

The command is written into the Control Word Registerand has the format shown in Figure below. Thecommand applies to the counters selected by setting their corresponding bits D3, D2, D1 = 1.

A0, A1 = 11; $\overline{CS}$ = 0 $\overline{RD}$ = 0 $\overline{WR}$ = 0

D7	D6	D5	D4	D3	D2	D1	D0
1	1	$\overline{count}$	$\overline{status}$	CNT-2	CNT-1	CNT-0	0

D5 : 0 Latch Count of selected counter(s)
D4 : 0 Latch status of selected counter(s)
D3 : 1 Select Counter 2
D2 : 1 Select Counter 1
D1 : 1 Select Counter 0
D0 : Reserved (must be '0')

Figure : Read-Back Command Format

The read-back command may be used to latch multiplecounter output latches (OL) by setting the COUNT bit D5 = 0 and selecting the desired counter(s). This single command is functionally equivalent to several counter latch commands, one foreach counter latched. Each counter's latched count is held until it is read (or the counter is reprogrammed). The counter is automatically unlatched when read, but other counters remain latched untilthey are read. Ifmultiple count read-back commands are issued to the same counter without reading thecount, all but the first are ignored; i.e., the countwhich will be read is the count at the time the firstread-back command was issued.

The read-back command may also be used to latchstatus information of selected counter(s) by setting STATUS bit D4 = 0. Status must be latched to beread; status of a counter is accessed by a read fromthat counter.

Figure : Status register							
D7	D6	D5	D4	D3	D2	D1	D0
O/P	NULL COUNT	RW1	RW0	M2	M1	M0	BCD

D7 : 1 = OUT Pin is 1
: 0 = OUT Pin is 0
D6 : 1 = Null Count
: 0 = Count Available for Reading
D5-D0 = Counter Programmed Mode

The counter status format is shown in Figure above. BitsD5 through D0 contain the counter'sprogrammedMode exactly as written in the last Mode ControlWord. OUTPUT bit D7 contains the current state ofthe OUT pin. This allows the user to monitor thecounter's output via software, possibly eliminatingsome hardware from a system.

Q. Explain various modes of 8254 programmable interval timer/counter.

Mode Definitions

The following are defined for use in describing theoperation of the 8254.

CLK Pulse : A rising edge, then a falling edge, inthat order, of a Counter's CLK input.

Trigger : A rising edge of a Counter's GATEinput.

Counter loading: The transfer of a count from the CRto the CE (refer to the ``FunctionalDescription'')

MODE 0: INTERRUPT ON TERMINAL COUNT

Mode 0 is typically used for event counting. After theControl Word is written, OUT is initially low, and willremain low until the Counter reaches zero. OUT then goes high and remains high until a new count or anew Mode 0 Control Word is written into the Counter.

GATE = 1 enables counting; GATE = 0 disablescounting. GATE has no effect on OUT.

After the Control Word and initial count are written toa Counter, the initial count will be loaded on the nextCLK pulse. This CLK pulse does not decrement thecount, so for an initial count of N, OUT does not gohigh until N a 1 CLK pulses after the initial count is written.

If a new count is written to the Counter, it will beloaded on the next CLK pulse and counting will continuefrom the new count. If a two-byte count is written,the following happens:

1) Writing the first byte disables counting. OUT is setlow immediately (no clock pulse required)

2) Writing the second byte allows the new count tobe loaded on the next CLK pulse.

This allows the counting sequence to be synchronizedby software. Again, OUT does not go high untilN+1 CLK pulses after the new count of N is written.

If an initial count is written while GATE = 0, it willstill be loaded on the next CLK pulse. When GATEgoes high, OUT will go high N CLK pulses later; no CLK pulse is needed to load the Counter as this hasalready been done.

MODE 1: HARDWARE RETRIGGERABLEONE-SHOT

OUT will be initially high. OUT will go low on the CLKpulse following a trigger to begin the one-shot pulse,and will remain low until the Counter reaches zero.OUT will then go high and remain high until the CLKpulse after the next trigger.

After writing the Control Word and initial count, theCounter is armed. A trigger results in loading theCounter and setting OUT low on the next CLK pulse, thus starting the one-shot pulse. An initial count of Nwill result in a one-shot pulse N CLK cycles in duration.
The one-shot is retriggerable, hence OUT willremain low for N CLK pulses after any trigger. Theone-shot pulse can be repeatedwithout rewriting thesame count into the counter. GATE has no effect onOUT.
If a new count is written to the Counter during aoneshotpulse, the current one-shot is not affected unlessthe counter is retriggered. In that case, theCounter is loaded with the new count and the oneshotpulse continues until the new count expires.

MODE 2: RATE GENERATOR

This Mode functions like a divide-by-N counter. It istypically used to generate a Real Time Clock interrupt.OUT will initially be high. When the initial counthas decremented to 1, OUT goes low for one CLKpulse. OUT then goes high again, the Counter reloads
the initial count and the process is repeated.Mode 2 is periodic; the same sequence is repeatedindefinitely. For an initial count of N, the sequencerepeats every N CLK cycles.

GATE = 1 enables counting; GATE e = disablescounting.

If GATE goes low during an output pulse,OUT is set high immediately. A trigger reloads theCounter with the initial count on thenext CLK pulse; OUT goes low N CLK pulses after the trigger. Thusthe GATE input can be used to synchronize theCounter.
After writing a Control Word and initial count, theCounter will be loaded on the next CLK pulse. OUTgoes low N CLK Pulses after the initial count is written.This allows the Counter to be synchronized bysoftware also.
Writing a new count while counting does not affectthe current counting sequence. If a trigger is receivedafter writing a new count but before the endof the current period, the Counter will be loaded withthe new count on the next CLK pulse and counting
will continue from the new count. Otherwise, thenew count will be loaded at the end of the currentcounting cycle. In mode 2, a COUNT of 1 is illegal.

MODE 3: SQUARE WAVE MODE

Mode 3 is typically used for Baud rate generation.Mode 3 is similar to Mode 2 except for the duty cycleof OUT. OUT will initially be high. When half theinitial count has expired, OUT goes low for the remainderof the count. Mode 3 is periodic; the sequenceabove is repeated indefinitely. An initialcount of N results in a square wave with a period ofN CLK cycles.
GATE = 1 enables counting; GATE e 0 disablescounting. If GATE goes low while OUT is low, OUT isset high immediately; no CLK pulse is required. Atrigger reloads the Counter with the initial count onthe next CLK pulse. Thus the GATE input can beused to synchronize the Counter.After writing a Control Word and initial count, theCounter will be loaded on the next CLK pulse. Thisallows the Counter to be synchronized by softwarealso.
Writing a new count while counting does not affectthe current counting sequence. If a trigger is receivedafter writing a new count but before the endof the current half-cycle of the square wave, theCounter will be loaded with the new count on thenext CLK pulse and counting will continue from thenew count. Otherwise, the new count will be loadedat the end of the current half-cycle.
Mode 3 is implemented as follows:
Even counts: OUT is initially high. The initial count isloaded on one CLK pulse and then is decrementedby two on succeeding CLK pulses. When the countexpires OUT changes value and the Counter is reloadedwith the initial count. The above process isrepeated indefinitely.
Odd counts: OUT is initially high. The initial count minus one (an even number) is loaded on one CLKpulse and then is decremented by two on succeedingCLK pulses. One CLK pulse after the count expires,OUT goes low and the Counter is reloadedwith the initial count minus one. Succeeding CLKpulses decrement the count by two. When the countexpires, OUT goes high again and the Counter isreloaded with the initial count minus one. The aboveprocess is repeated

indefinitely. So for odd counts,OUT will be high for (N + 1)/2 counts and low for(N + 1)/2 counts.

MODE 4: SOFTWARE TRIGGERED STROBE

OUT will be initially high. When the initial count expires,OUT will go low for one CLK pulse and thengo high again. The countingsequence is ``triggered"by writing the initial count.

GATE = 1 enables counting; GATE = 0 disablescounting. GATE has no effect on OUT.

After writing a Control Word and initial count, theCounter will be loaded on the next CLK pulse. ThisCLK pulse does not decrement the count, so for aninitial count of N, OUT does not strobe low until N + 1 CLK pulses after the initial count is written.

If a new count is written during counting, it will beloaded on the next CLK pulse and counting will continuefrom the new count. If atwo-byte count is written,the following happens:

1) Writing the first byte has no effect on counting.

2) Writing the second byte allows the new count tobe loaded on the next CLK pulse.

This allows the sequence to be ``retriggered" bysoftware. OUT strobes low N a 1 CLK pulses afterthe new count of N is written.

MODE 5: HARDWARE TRIGGERED STROBE (RETRIGGERABLE)

OUT will initially be high. Counting is triggered by arising edge of GATE. When the initial count has expired,OUT will go low for one CLK pulse and thengo high again.

After writing the Control Word and initial count, thecounter will not be loaded until the CLK pulse after atrigger. This CLK pulse does not decrement thecount, so for an initial count of N, OUT does notstrobe low until N + 1 CLK pulses after a trigger.A trigger results in the Counter being loaded with theinitial count on the next CLK pulse. The countingsequence is retriggerable. OUT will not strobe lowfor N + 1 CLK pulses after any trigger. GATE hasno effect on OUT.

If a new count is written during counting, the currentcounting sequence will not be affected. If a triggeroccurs after the new count is written but before thecurrent count expires, the Counter will be loadedwith the new count on the next CLK pulse andcounting will continue from there.